ABSTRACT

METHOD FOR PROVIDING A CELL-BASED ASIC DEVICE WITH MULTIPLE POWER SUPPLY VOLTAGES

A method for designing a cell-based ASIC device with multiple power supply voltages is disclosed. An ASIC chip image is made without applying power or ground buses to metal layer M1. All fast or high-power circuits are grouped together into high-power logic blocks and synthesized with high-power circuit macro libraries. All slow or low-power circuits are grouped together into low-power logic blocks and synthesized with low power circuit macro libraries. The associate power and ground buses are applied to metal layer M1 in each of the logic blocks. The logic blocks are placed on the ASIC so that different voltage groups are separated by at least one cell. The ASIC is then routed and tested before the mask is released.